UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/887,560	06/25/2001	Edward Colles Nevill	550-243	7549

23117 7590 06/30/2004

NIXON & VANDERHYE, PC
1100 N GLEBE ROAD
8TH FLOOR
ARLINGTON, VA 22201-4714

EXAMINER	
O BRIEN, BARRY J	
ART UNIT	**PAPER NUMBER**
2183	10

DATE MAILED: 06/30/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/887,560	Applicant(s) NEVILL ET AL.	
	Examiner Barry J. O'Brien	Art Unit 2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *6/25/01 to 3/31/04*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *8, 9*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-17 have been examined.

Papers Submitted

2. It is hereby acknowledged that the following papers have been received and placed on record in the file: Priority Papers as received on 10/11/01, Copy of Specification and Drawings as received on 10/11/01, IDS as received on 10/11/01, Declaration and Fee as received on 10/16/01, Pre-Amendment A as received on 6/25/01, Change of Address as received on 3/31/04, and IDS as received on 3/31/04.

Specification

3. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

4. The applicant is requested to review the specification and update the status of all co-pending applications made mention of, replacing attorney docket numbers with current U.S. application or patent numbers when appropriate.

5. The abstract of the disclosure is objected to because of the following informalities:

   a. The abstract contains reference numerals 102, 104, 106 and 108. Because it is an abstract, it is unclear what the reference numerals correspond to. Please remove the reference numerals from the abstract.

b. The abstract contains a line reciting, "[Figure 6]". It is unclear why this phrase is in the abstract, as no figure is present. Please remove the above phrase from the abstract.

Correction is required. See MPEP § 608.01(b).

Claim Objections

6. Claim 17 is objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Applicant is required to cancel the claim(s), or amend the claim(s) to place the claim(s) in proper dependent form, or rewrite the claim(s) in independent form.

7. Claims 17 recites the limitation, "A computer program product holding a computer program for controlling a computer to perform the method of claim 16". The parent claim of claim 17, claim 16, already claims a processor (processor core) that executes instructions to control it, instructions which inherently reside on some sort of computer readable medium (computer program product). Therefore, because there is no way that the processor core of claim 16 can function as claimed without the instructions that execute on the processor core being comprised on a computer program product, claim 17 fails to further limit the subject matter of claim 16.

8. Claim 1-16 are objected to because of the following informalities:

a. Claim 1 recites the limitation, "Apparatus for processing data" in its preamble. Please amend the claim language to read, "An apparatus for processing data" in

order to be more grammatically correct. The same correction needs to also be made for dependent claims 2-15.

b. Claim 14 recites the limitation, "a second plurality of state bits". It is unclear what why a "first plurality of state bits" was not claimed in parent claims 1 and 5. Please correct this claim language to more clearly read "a first plurality of state bits", or change the parent claim to be, for example, claim 13, which does in fact recite the limitation "a first plurality of state bits."

c. Claim 16 recites the limitation, "changing between mapping states" on its second to last line. Please correct this claim language to more clearly read, "changing between said plurality of mapping states".

d. A series of singular dependent claims is permissible in which a dependent claim refers to a preceding claim which, in turn, refers to another preceding claim. A claim that depends from a dependent claim should not be separated by any claim that does not also depend from said dependent claim. It should be kept in mind that a dependent claim may refer to any preceding independent claim. In general, applicant's sequence will not be changed. See MPEP § 608.01(n). See claims 5-15, where claim 14 improperly depends on claim 5, while claims 13 and 15 depend on claim 1.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

9. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

10. Claim 3 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

11. Claim 3 recites the limitation, "said translator output signals include control signals that control operation of said processor core and match signals produced on decoding instructions of said first instruction set". It is unclear whether "match signals" refers to a separate group of signals of the translator output signals simply called "match signals", or if it refers to the "control signals" being equal to signals "produced on decoding instructions of a said first instruction set". Please correct the claim language to more clearly define the metes and bounds of the invention. For the purposes of this examination, the Examiner will assume that "match signals" refer to "control signals" being equal to signals "produced on decoding instruction of a said first instruction set".

Claim Rejections - 35 USC § 102

12. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

13. Claims 1-17 are rejected under 35 U.S.C. 102(e) as being anticipated by Patel et al., U.S. Patent No. 6,332,215.

14. Regarding claim 1, Patel has taught an apparatus for processing data, said apparatus comprising:

a. A processor core (26 of Fig.1) having a register bank (48 of Fig.3) containing a plurality of registers and being operable to execute operations upon register operands held in said registers as specified within instructions of a first instruction set (see Col.4 lines 46-54),

b. An instruction translator (42 of Fig.3) operable to translate instructions of a second instruction set into translator output signals corresponding to instructions of said first instruction set (see Col.4 lines 1-4), instructions of said second instruction set specifying operations to be executed upon stack operands held in a stack (see Col.2 lines 19-21),

c. Wherein said instruction translator is operable to allocate a set of registers within said register bank to hold stack operands from a portion of said stack (see Col.4 lines 46-54 and Col.6 lines 1-11),

d. Said instruction translator has a plurality of mapping states in which different registers within said set of registers hold respective stack operands from different positions within said portion of said stack (see Col.4 lines 6-22 and Col.5 line 48 – Col.6 line 11).

e. Said instruction translator is operable to change between mapping states in dependence upon operations that add or remove stack operands held within said set of registers (see Col.4 lines 6-22 and Col.5 line 48 – Col.6 line 11).

15. Regarding claim 2, Patel has taught an apparatus as claimed in claim 1, wherein said translator output signals include signals forming an instruction of said first instruction set (see Col.4 lines 1-4).

16. Regarding claim 3, Patel has taught an apparatus as claimed in claim 1, wherein said translator output signals include control signals that control operation of said processor core and match control signals produced on decoding instructions of said first instruction set (see Col.2 line 65 – Col.3 line 5). Here, native instructions, which are control signals that control the processing core, are the same whether they were translated from Java bytecodes or not when being passed to the processor core (see Fig. 3).

17. Regarding claim 4, Patel has taught an apparatus as claimed in claim 1, wherein said translator output signals include control signals that control operation of said processor core and specify parameters not specified by control signals produced on decoding instructions of said first instruction set (see Col. 5 lines 43-47). Here, non-translated instructions will not access the instruction translator (see Fig.3), and thus will not produce output to the Java Registers (44 of Fig.4).

18. Regarding claim 5, Patel has taught an apparatus as claimed in claim 1, wherein said instruction translator provides mapping states such that stack operands are added to or removed from said set of registers without moving stack operands between registers within said set of registers (see Col.5 line 48 – Col.6 line 11).

19. Regarding claim 6, Patel has taught an apparatus as claimed in claim 1, wherein said set of registers are operable to hold stack operands from a top portion of said stack including a top of stack operand form a top position within said stack (see Col.4 lines 6-22).

20. Regarding claim 7, Patel has taught an apparatus as claimed in claim 1, wherein said stack further comprises a plurality of addressable memory locations holding stack operands (see Col.4 lines 12-15).

21. Regarding claim 8, Patel has taught an apparatus as claimed in claim 7, wherein stack operands overflow from said set of registers into said plurality of addressable memory locations (see Col.4 lines 54-60 and Col.6 lines 1-24).

22. Regarding claim 9, Patel has taught an apparatus as claimed in claim 7, wherein stack operands held within said plurality of addressable memory locations are loaded into said set of registers prior to use (see Col.4 lines 54-60 and Col.6 lines 1-24).

23. Regarding claim 10, Patel has taught an apparatus as claimed in claim 1, wherein said instruction translator uses a plurality of instruction templates (78 of Fig.4) for translating instructions from said second instruction set to instructions from said first instruction set (see Col.5 lines 30-42).

24. Regarding claim 11, Patel has taught an apparatus as claimed in claim 10, wherein an instruction from said second instruction set including one or more stack operands has an instruction template comprising one or more instructions from said first instruction set in which register operands are mapped to said stack operands (see Col.5 lines 30-60).

25. Regarding claim 12, Patel has taught an apparatus as claimed in claim 1, wherein said instruction translator comprises one or more of:

a. Hardware translation logic (42 of Fig.3),

b. Instruction interpreting program code controlling a computer apparatus,

c. Instruction compiling program code controlling a computer apparatus,

d. Hardware compiling logic.

26. Because the claim is written in the alternative format, only one of the four possible alternatives has to be met, and thus Patel has taught the limitations of the claim.

27. Regarding claim 13, Patel has taught an apparatus as claimed in claim 1, wherein said instruction translator includes a first plurality of state bits indicative of a number of stack operands held within said set of registers (see Col.5 lines 34-47). Here, there are counters that keep track of the number of entries on the stack (see Col.5 lines 34-37), and the stack is held in the set of registers with the translator keeping track of the arrangement of the stack in the registers (see Col.5 lines 43-47).

28. Regarding claim 14, Patel has taught an apparatus as claimed in claim 5, wherein said instruction translator includes a second plurality of state bits indicative of which register within said set of registers holds said top of stack operand (see Col.4 lines 6-22).

29. Regarding claim 15, Patel has taught an apparatus as claimed in claim 1, wherein said second instruction set is a Java Virtual Machine Instruction set (see Col.2 lines 60-63).

30. Regarding claim 16, Patel has taught a method of processing data using a processor core (26 of Fig.1) having a register bank (48 of Fig.3) of containing a plurality of registers and being operable to execute operations upon register operands held in said registers as specified within instructions of a first instruction set (see Col.4 lines 46-54), said method comprising the steps of:

a. Translating instructions of a second instruction set into translator output signals corresponding to instructions of said first instruction set (see Col.4 lines 1-4), instructions of said second instruction set specifying operations to be executed upon stack operands held in a stack (see Col.2 lines 19-21),

b. Allocating a set of registers within said register bank to hold stack operands from a portion of said stack (see Col.4 lines 46-54 and Col.6 lines 1-11),

c. Adopting one of a plurality of mapping states in which different registers within said set of registers hold respective stack operands from different positions within said portion of said stack (see Col.4 lines 6-22 and Col.5 line 48 – Col.6 line 11),

d. Changing between mapping states in dependence upon operations that add or remove stack operands held within said set of registers (see Col.4 lines 6-22 and Col.5 line 48 – Col.6 line 11).

31. Regarding claim 17, Patel has taught a computer program product holding a computer program for controlling a computer to perform the method of claim 16 (see Col.2 line 65 – Col.3 line 5).

Conclusion

32. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Applicant is reminded that in amending in response to a rejection of claims, the patentable novelty must be clearly shown in view of the state of the art disclosed by the references cited and the objections made. Applicant must also show how the amendments avoid such references and objections. See 37 CFR § 1.111(c).

33. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Barry J. O'Brien whose telephone number is (703) 305-5864. The examiner can normally be reached on Mon.-Fri. 6:30am-4:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (703) 305-9712. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

34. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Barry J. O'Brien
Examiner
Art Unit 2183

BJO
6/25/2004

EDDIE CHAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100